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(54) Voltage regulator with load pole stabilization

(57) A voltage regulator with load pole stabilization is disclosed. The voltage regulator consists of an error amplifier, an integrator which includes a switched capacitor, a pass transistor, and a feed back circuit. In one embodiment, the integrator circuit includes an amplifier, a capacitor, and a switched capacitor which is driven by a voltage controlled oscillator. The voltage controlled oscillator changes its frequency of oscillation proportional to the output current. In another embodiment, the switched capacitor is driven by a current controlled oscillator whose frequency of oscillation is also proportional to the output current of the voltage regulator. When the output current demand is large, the controlled oscillators increase the frequency which decreases the effective resistance of the switched capacitor thereby changing the frequency of the zero to respond to the change in the load pole. Conversely, the effective resistance is increased as the current demand is decreased, also to respond to the decrease in load pole. Consequently, the disclosed voltage regulator has high stability without consuming excess power.

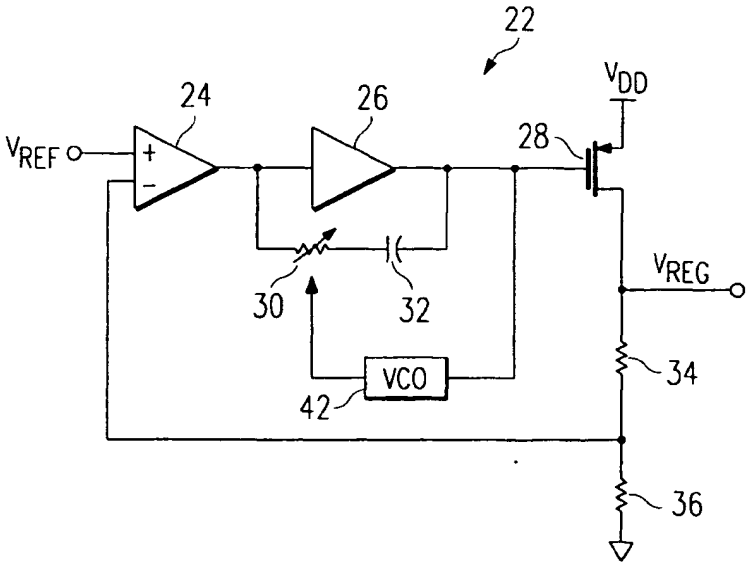

FIG. 2

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Description

This invention relates to electronic circuits used as voltage regulators and more specifically to circuits and methods used to stabilize a voltage regulator.

The problem addressed by this invention is encountered in voltage regulation circuits. Voltage regulators are inherently medium to high gain circuits, typically greater than 50db, with low bandwidth. With this high gain and low bandwidth, stability is often achieved by setting a dominate pole set with the load capacitor. Achieving stability over a wide range of load currents with a low value load capacitor (-O.luF) is difficult because the load pole formed by the load capacitor and load resistor can vary by more than three decades of frequency and be as high as tens of KHz requiring the circuit to have a very broad bandwidth of greater than 3MHz which is incompatible with the power process used for voltage regulators.

Figure 1 shows a prior art solution to the stabilization problem. The voltage regulator 2 in Fig. 1 converts an unregulated Vdd voltage, 12 volts in this example, into a regulated voltage Vreg, 5 volts in this example. Amplifier 6, resistor 10, and capacitor 12 are configured as an integrator thereby providing a zero to cancel the pole of the load (load pole). The integrator drives pass transistor 8. Resistors 14 and 16 form a voltage divider circuit which is used to scale the output voltage such that the output voltage can be fed back to the inverting input of an error amplifier 4. Resistor 18 and capacitor 20 are not part of voltage regulator 2 but rather are the schematic representation of the typical load on the voltage regulator circuit.

In this prior art example, the pole associated with the load can be calculated as:

$$f_{pole} = \frac{1}{2\Pi C_L R_L}$$

where R_L = resistance of the load.

C_L = is the capacitance of C20 which is typically around .1 microfarad.

Therefore, the pole associated with the prior art circuit is load dependent and can vary from 16 Hz to 32 KHz for an R14 + R16 equal to 100 kilo-ohms and R18 ranging from 50 ohms to 1 mega-ohm. The wide variation of the pole frequency is difficult to stabilize, as will be appreciated by persons skilled in the art. A prior art solution to this problem is to change the pull down resistors R14 + R16 from 500 kilo-ohms to around 500 ohms which changes the pole frequency to a range of 3.2 KHz to 32 KHz, which is a frequency spread of 1 decade instead of 3 decades. However, the power dissipated by the pull down resistor R18 increases, as shown below:

$$\text{power} = (12v\text{-}5v)(I_{load} + I_{pull\ down}) = (7v)(100mA)+(7v)(10mA)$$

Therefore, the 500 ohm resistor adds 70 milli-watts of power dissipation in the chip which is approximately a 10% increase in power dissipation for the added stability.

Therefore, it is an object of the invention to increase the stability of a voltage regulator without increasing the power dissipated in the circuit. Additionally, it is an object of the invention to have a load cancelling zero which follows the load pole. Further, it is an object of the invention to have an integration circuit which has a load cancelling zero (cancellation zero) which varies with load pole. These and other objects, features, and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read with the drawings and claims.

The invention can be summarized as a voltage regulator with load pole stabilization. The voltage regulator consists of an error amplifier, an integrator which includes a switched capacitor, a pass transistor, and a feed back circuit. In one embodiment, the integrator circuit includes an amplifier, a capacitor, and a switched capacitor which is driven by a voltage controlled oscillator. The voltage controlled oscillator changes its frequency of oscillationas a function of the output current of the voltage regulator. In another embodiment, the switched capacitor is driven by a current controlled oscillator whose frequency of oscillation is also a function of the output current of the voltage regulator. When the output current demand is large, the controlled oscillators increase the frequency of oscillation which decreases the effective resistance of the switched capacitor, thereby changing the frequency of the cancellation zero to respond to the change in the load pole. Conversely, the effective resistance is increased as the current demand is decreased, also to respond to the decrease in load pole. Consequently, the disclosed voltage regulator has high stability without consuming excess power.

Some embodiments of the invention will now be described by way of example and with reference to the accom-

panying drawings in which:

Fig. 1 is a schematic diagram of a voltage regulator as is known in the prior art.

Fig. 2 is a schematic diagram of a voltage regulator with a switched capacitor, driven by a voltage control oscillator, in the integrator circuit.

Fig. 3 is a schematic diagram of a switched capacitor as known in the prior art.

Fig. 4 is a timing diagram describing the operation of a switched capacitor.

Fig. 5 is a schematic diagram of a voltage sense circuit which can be used in conjunction with a voltage control oscillator.

Fig. 6 is another embodiment of a voltage regulator with a switched capacitor driven by a current controlled oscillator.

A voltage regulator constructed according to the embodiment of the invention in Figure 2 will now be described. Error amplifier 24 has a noninverting input for receiving a Vref voltage. The output of error amplifier 24 is coupled to the integrator circuit and more specifically to the input of amplifier 26 and to the first end of switched capacitor 30. The second end of switched capacitor 30 is coupled to the first end of capacitor 32. The second end of capacitor 32 is connected to the output of amplifier 26, the gate of P-channel MOSFET pass transistor 28 and the input of voltage controlled oscillator 42. The output of the voltage control oscillator 42 is coupled to the input of the switched capacitor 30. The source of pass transistor 28 is connected to a voltage source Vdd. The drain of pass transistor 28 forms the output of voltage regulator 22 and is connected to the first end of resistor 34. The second end of resistor 34 is connected to the first end of resistor 36 and the inverting input of error amplifier 24. The second end of resistor 36 is connected to ground.

In operation, the reference voltage Vref is compared to the regulated voltage Reg through the feedback circuit formed by resistor 34 and resistor 36. More specifically, resistors 34 and 36 are configured as a voltage divider to scale the Vreg voltage which is then fed back to the inverting input of the error amplifier.

The integrator formed by amplifier 26, switched capacitor 30 and capacitor 32 has a zero with a frequency at

$$f_{zero} = \frac{1}{2\pi C_{32} R_{eff}}$$

where

$$R_{eff} = \frac{1}{f_{vco} C_{30}}$$

Thus, the pass transistor 28 regulates the Vreg voltage responsive to the error amplifier 24 and integrator output.

Figure 2 also shows the switched capacitor 30 being switched at a frequency controlled by the voltage control oscillator 42. The input to the voltage control oscillator 42 is connected to the output of the integrator circuit. The operation of this circuit can be described with the following equations:

$$f_{pole} = \frac{1}{2\Pi R_L C_L}$$

$$f_{zero} = \frac{1}{2\Pi C_{32} R_{eff}}$$

By setting the load pole frequency equal to the zero frequency and solving for the VCO frequency, we obtain:

$$f_{VCO} = \frac{C_{32}}{C_{30}} \frac{1}{R_L C_L}$$

and,

$$f_{VCO} = \frac{C_{32}}{C_{30}} \frac{I_{load}}{V_{reg}} \frac{1}{C_L}$$

Therefore, the VCO frequency is proportional to the switching capacitor C32 and to the output current in this example. Thus, the cancellation zero generated by the integrator follows the load pole as the load changes. Persons skilled in the art will be able to utilize these equations to design a voltage regulator which meets their design criteria.

The invention increases the stability of the voltage regulator 22 without increasing the power dissipated by the circuit. This is accomplished by having a load cancelling zero which follows the load pole without having use low resistance pull down resistors which dissipate excessive power, as described above.

The construction of a switched capacitor as illustrated in Figure 3 will now be described. Figure 3 shows switched capacitor having a first end connected to the drain of MOSFET transistor 40 and the drain of MOSFET transistor 42 and having a second end connected to ground. The source of transistor 40 forms the input to the switched capacitor and the source of transistor 42 forms the output of the switched transistor. The gate of transistor 40 is shown to receive a signal ϕ while the gate of transistor 42 is shown to receive the inverted signal ϕbar. It will be understood by persons skilled in the art that transistors 40 and 42, although shown as N-channel transistors, could be P-channel MOSFETs, bipolar transistors, or any equivalent thereof.

Figure 4 shows the input timing signals as well as the effective resistance of the circuit as a function of frequency. Figure 4a shows the input waveform ϕ which would be applied to the gate of transistor 40. Figure 4b shows the timing waveform for the signal ϕ bar which would go on the input of transistor 42. It should be noted that these are non-overlapping waveforms. Therefore, transistor 40 is never on at the same time that transistor 42 is on. Figure 4c shows that the effective resistance R_{eff} of the switched capacitor decreases as the frequency increases. Conversely, the effective resistance R_{eff} increases as frequency decreases.

Figure 5 illustrates a circuit which provides a voltage which is proportional to the output current of the voltage regulator. The circuit in Figure 5 provides an alternative embodiment to the method for driving the VCO in Figure 2.

More specifically, Figure 5 shows a pass transistor 44 connected in series with a sense resistor Rsense to generate a voltage which can be used by a VCO. Figure 5 is shown as an alternative to connecting the VCO to the gate of the pass transistor 28 in Figure 2. Further, Figure 5 shows the first end of the resistor Rsense connected to the source of pass transistor 48. The second end of Rsense forms the output of the voltage regulator and is coupled to the first end of resistor 54. The second end of resistor 54 is connected to first end of resistor 56. The second end of resistor 56 is connected to ground. It will be appreciated by persons skilled in the art that Rsense would be selected such that the voltage drop across Rsense is minimized.

With Rsense configured in this manner, a voltage Vsense is generated which is proportional to the output current of the voltage regulator. This voltage can subsequently be used to drive the VCO.

Yet another embodiment is shown in Figure 6. The embodiment in Figure 6 differs from the embodiment in Figure 2 in that the switched capacitor 70 is controlled by a current controlled oscillator (ICO) whereas the switched capacitor 30 in Figure 2 is controlled by a voltage control oscillator.

The voltage regulator in Figure 6 is constructed by having an error amplifier 64 receive a reference voltage Vref into its noninverting input. The output of the error amplifier 64 is connected to the input of amplifier 66 and to the first end of switched capacitor 70. The output of amplifier 66 is connected to a gate of P-channel transistor 82 and the gate of P-channel transistor 68 and the second end of capacitor 72. The first end of capacitor 72 is connected to the second end of switched capacitor 70. The frequency input of switched capacitor 70 is connected to the output of ICO 80. The input of ICO 80 is connected to the drain of transistor 82. The drain of transistor 68 forms the output of the voltage regulator and is connected to the first end of resistor 74. The second end of resistor 74 is connected to the inverting input of the error amplifier and the first end of resistor 76. The second end of resistor 76 is connected to ground.

The voltage regulator circuit in Figure 6 operates essentially the same way as the circuit in Figure 2. The difference between these two circuits is that the circuit in Figure 6 mirrors the output current by having the gate of transistor 82 connected to the gate of transistor 68. Therefore as the output current through transistor 68 increases, the current going into the ICO 80 also increases. As the current at the input of the ICO increases, the frequency coming out of the ICO and going into the switched capacitor 70 increases. Therefore, the resistance of switched capacitor 70 decreases. Like the circuit in Figure 2, the cancellation zero generated by the integrator follows the load pole as the load changes.

Therefore, the invention increases the stability of the voltage regulator 22 without increasing the power dissipated by the circuit. This is accomplished by having a load cancelling zero which follows the load pole.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

Claims

1. A voltage regulator circuit having an error amp, an integrator circuit, a pass transistor, and a feedback circuit, wherein the integrator circuit further comprises:

   an amplifier having an input and an output; and
   a switched capacitor and a capacitor coupled in series across the input and output of the amplifier.

2. A voltage regulator circuit comprising

   an error amp having a noninverting input for receiving a reference voltage, an inverting input, and an output;
   an integrator circuit comprising:
   an amplifier with an input coupled to the output of the error amp and having an output,
   a switched capacitor and a capacitor coupled in series across the input and output of the amplifier;
   a pass transistor having a current path with a first end coupled to a voltage source and a second end, and having a control element coupled to the output of the integrator circuit; and
   a feedback circuit coupled between the second end of the conductive path of the pass transistor and the inverting input of the error amplifier.

3. The voltage regulator circuit of claim 1 or claim 2, wherein the switched capacitor is switched at a frequency proportional to a current demand on the voltage regulator.

4. The voltage regulator circuit of claim 1 or claim 2, further comprising a voltage controlled oscillator having an input coupled to the output of the amplifier and having an output coupled to the switched capacitor.

5. The voltage regulator claim 1 or claim 2, further comprising a current controlled oscillator having an input coupled to the output of the amplifier and having an output coupled to the switched capacitor.

6. The voltage regulator of claim 1 or claim 2, wherein the switched capacitor comprises:

   a first transistor having a drain, source, and a gate for receiving a frequency from a variable frequency source;
   a capacitor having a first end coupled to the drain of the first transistor and having a second end coupled to ground; and
   a second transistor having a drain coupled to the first end of the capacitor, having a source, and having a gate for receiving an inverted signal from the variable frequency source.

7. The voltage regulator circuit of claim 6, wherein the variable frequency source comprises a voltage controlled oscillator or a current controlled oscillator.

8. The voltage regulator circuit of claim 6, wherein the first transistor and the second transistor are MOSFET transistors.

9. A method for stabilizing a regulating voltage with a load pole by generating a load pole cancelling zero comprising the steps of:

   generating a frequency inversely proportional to the load current; and
   driving a switched capacitor with the generated frequency.

10. The method of claim 9, wherein the step of generating a frequency is implemented using a voltage control oscillator.

11. The method of claim 9, wherein the step of generating a frequency is implemented using a current control oscillator.

12. A power supply which includes a voltage regulating circuit comprising:

    an error amp having a noninverting input for receiving a reference voltage, an inverting input, and an output,
    an integrator circuit comprising:
    an amplifier with an input coupled to the output of the error amp and having an output,
    a switched capacitor and a capacitor coupled in series across the input and output of the amplifier;

a pass transistor having a current path with a first end coupled to a voltage source and a second end, and having a control element coupled to the output of the integrator circuit; and

a feedback circuit coupled between the second end of the conductive path of the pass transistor and the inverting input of the error amplifier.

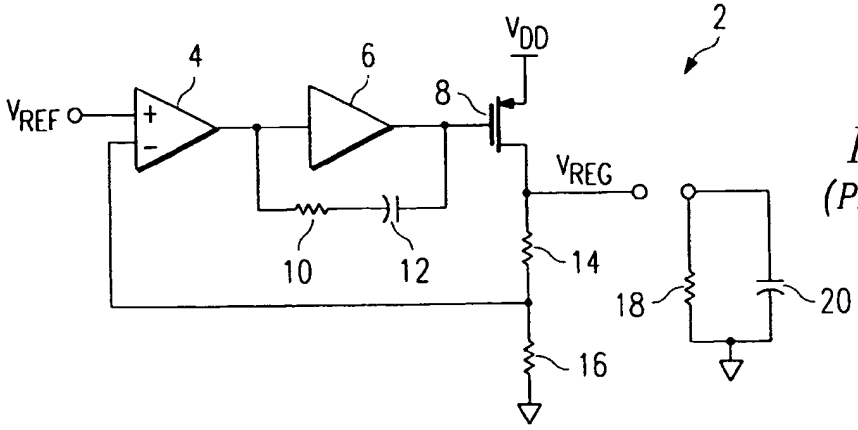

FIG. 1
(PRIOR ART)

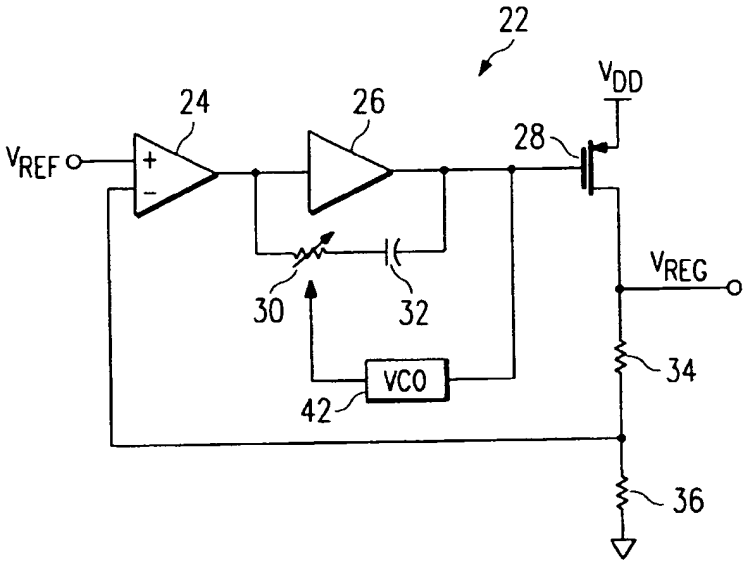

FIG. 2

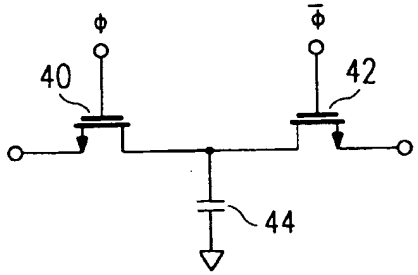

FIG. 3
(PRIOR ART)

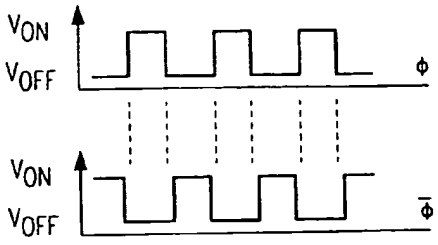

FIG. 4A

FIG. 4B

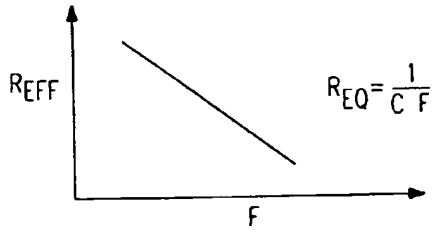

FIG. 4C

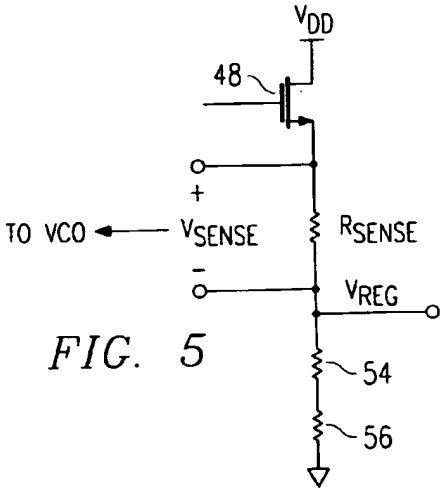

FIG. 5

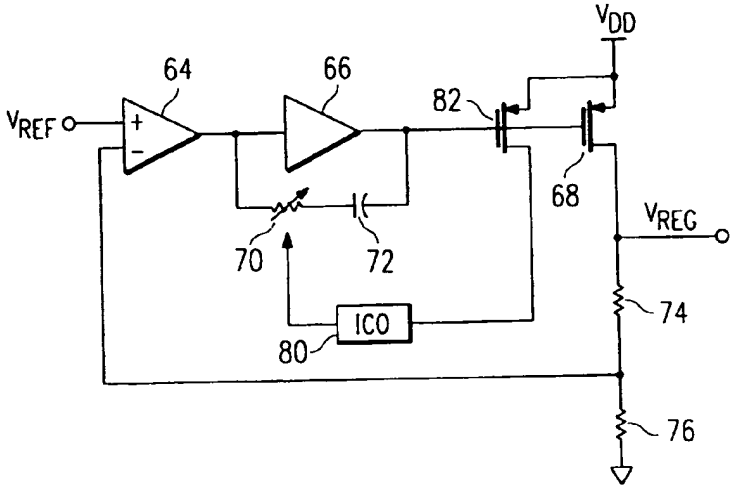

FIG. 6